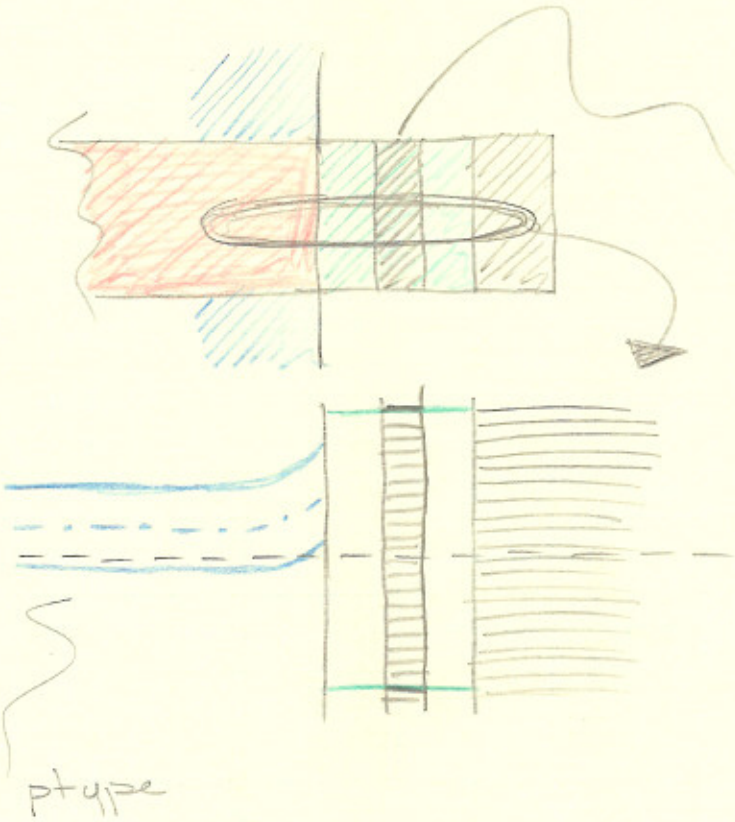
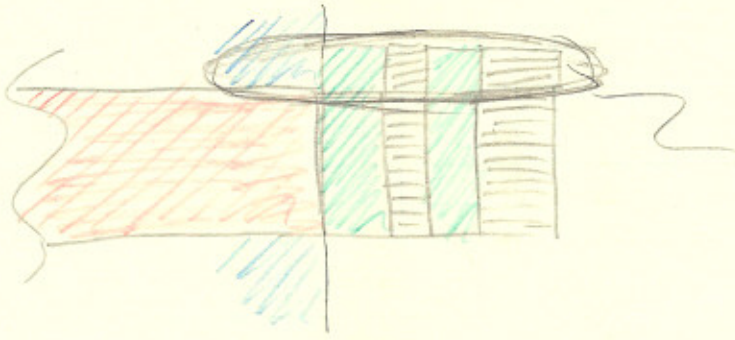
EPROM.

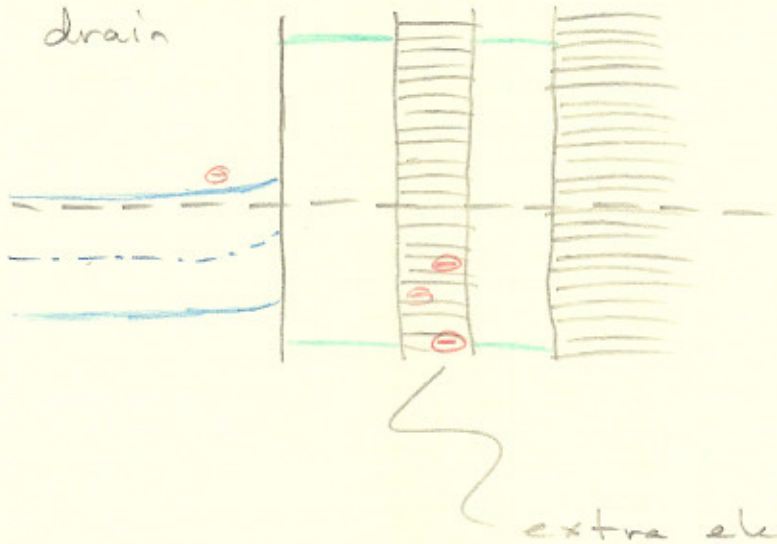
The main disadvantage of EPROM is that it needs to be removed from the circuit to be erraised.

EEPROM (electrically erraisable programable read only memory)



The dielectric and gates should be extended over part of the n^+ regain.



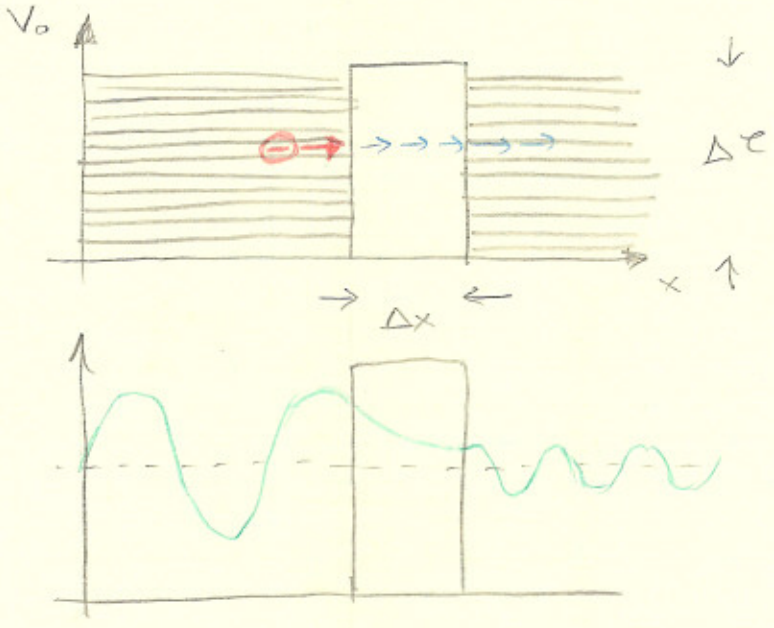


extra electrons are trapped in the floating gate giving it a negative charge

These extra electrons come for the n type material at the drain.

The electrons cross the dielectric layer by tunneling

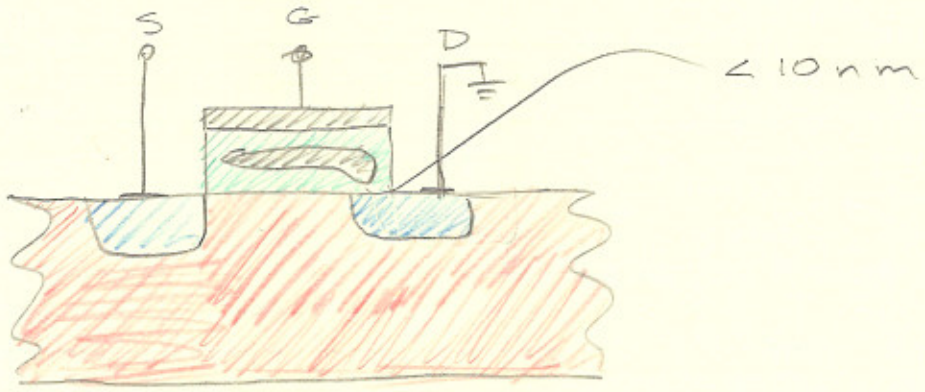
Tunneling



$\Delta e \cdot \Delta x < \hbar$

for the electron to pass

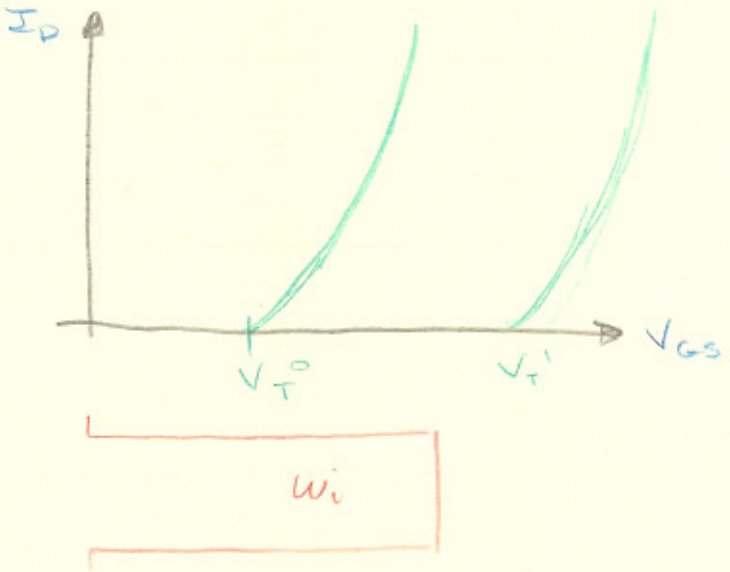
Hence we need to make sure that the width of the is not too large at the dialectric layer.



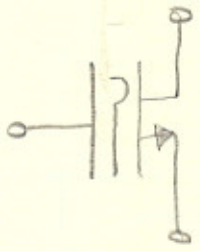
By make the gate 10V we create a feild strong enough to tunnel electrons into the floating gate

This charge is now stored in the floating gate

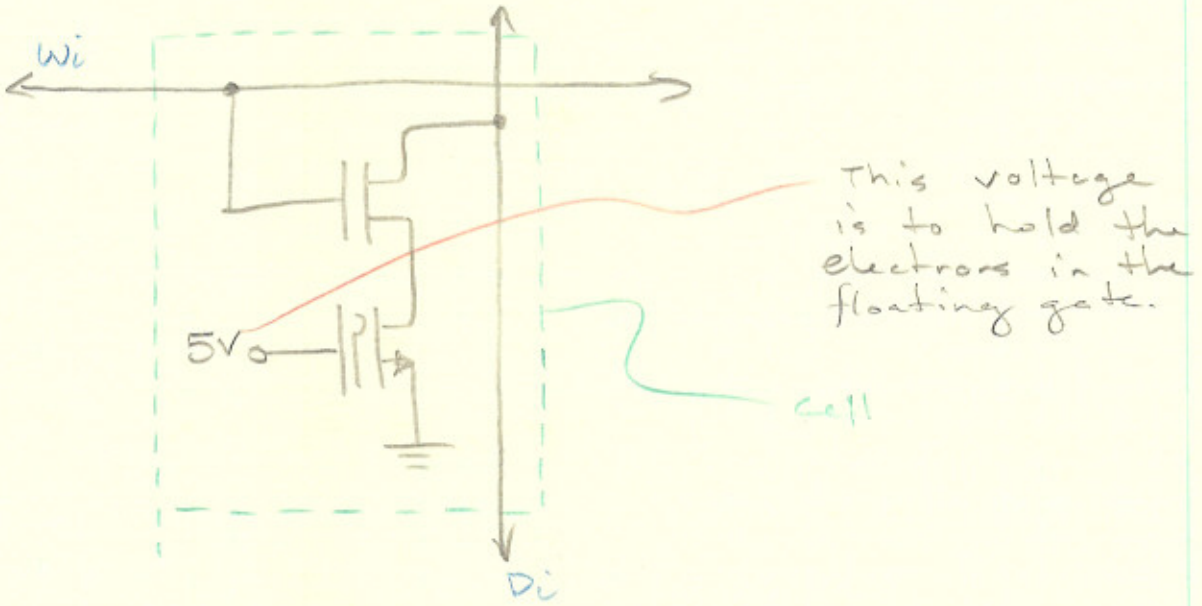
To remove the charge from the floating gate we apply a potential in the opposite way



The symbol for this transistor is....



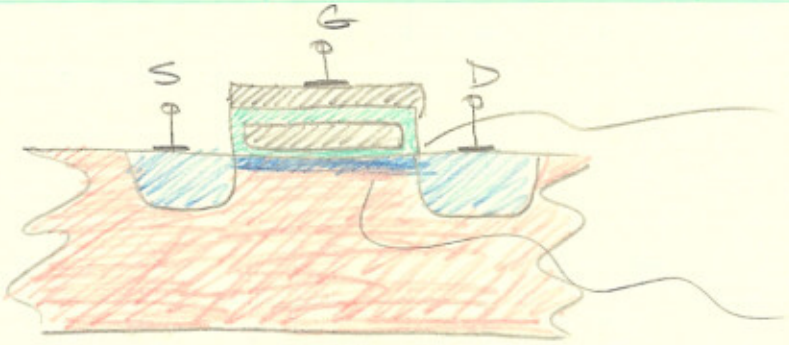
The corrispond cell hence is.



The cells are arranged in the standard ROM archatecture.

Flash EEPROM

Similiar to the EEPROM but the width to the floating gate is d/c and there is no over lap



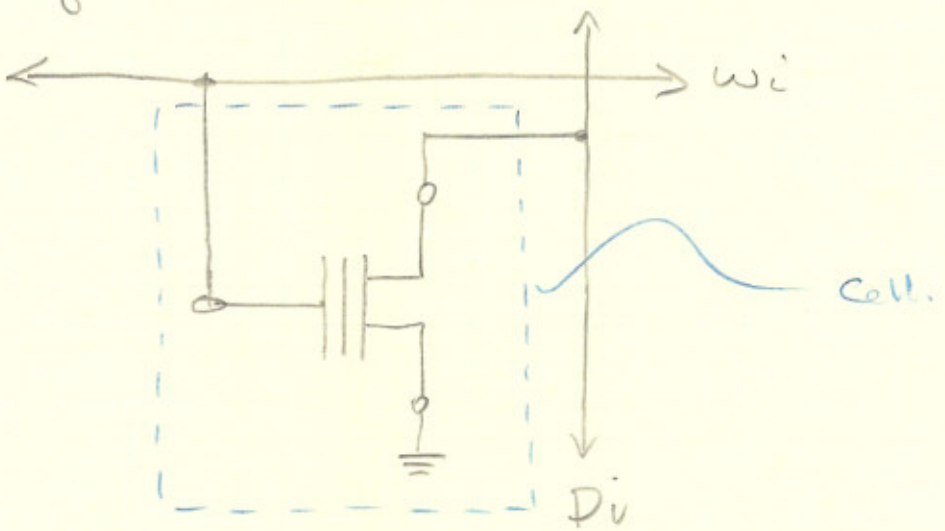
here we have 10 nm all the way across

note: this channel is only present during loading

By applying 12 V to the gate; grounding the source and and 6 V to the drain the electrons flow through the channel and some of them are trapped in the floating gate.

By applying 0 V to the gate and 6 V on the drain the electrons escape from the floating gate.

This technology is better made so that the electrons are guarentined in the floating gate. We do not need to apply a constant voltage



The cells are arranged in the standard ROM architecture.